

**FACULTATEA DE AUTOMATICĂ ŞI CALCULATOARE**

**~SPECIALIZAREA: CALCULATOARE SI TEHNOLOGIA INFORMATIEI~**

RAPORT MIPS 16

PIPELINE

**Student: Arseniuc Anamaria**

**Grupa 30226**

**An 2, Semestrul 2**

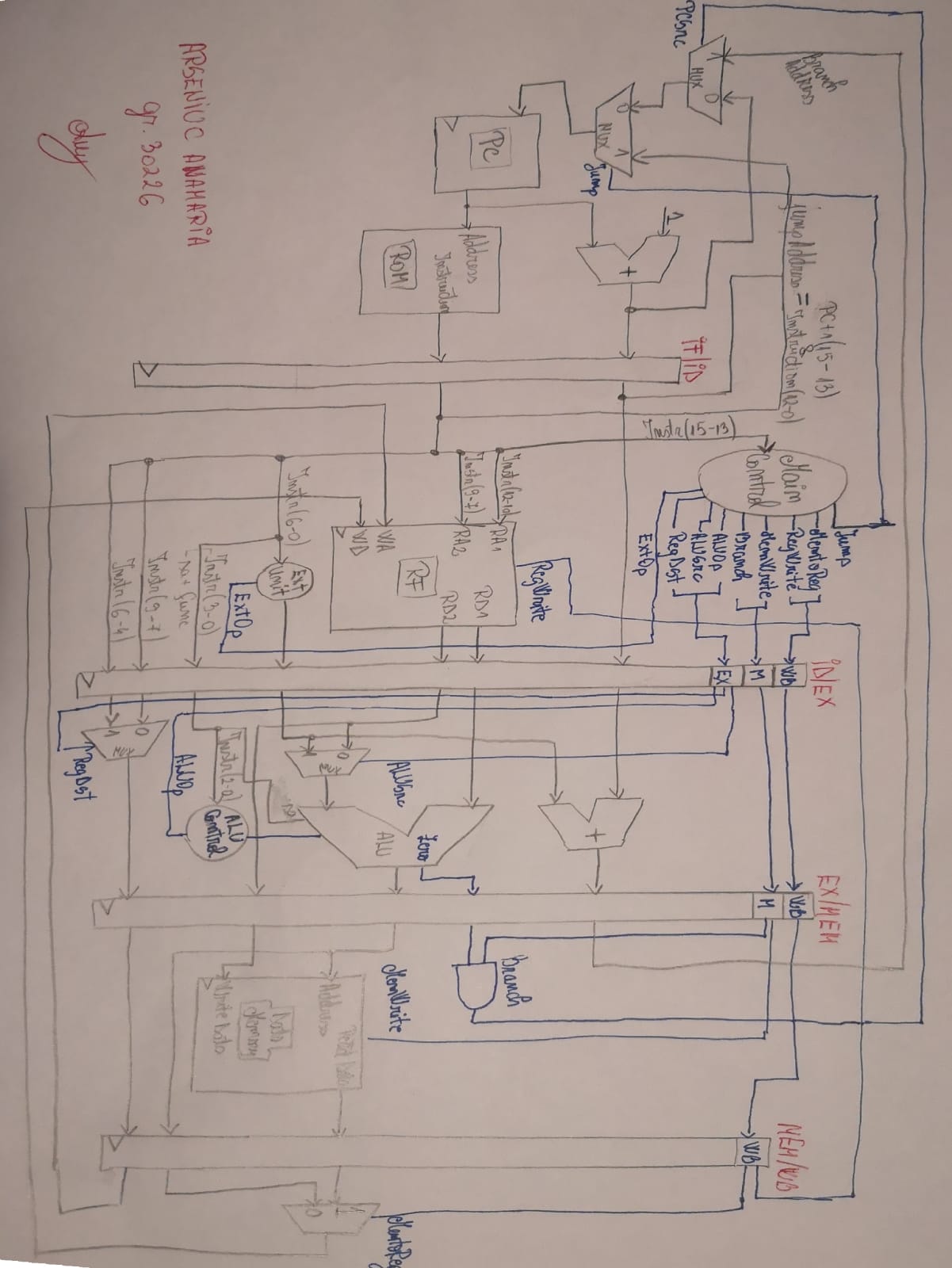
**Configurare registre MIPS16 Pipeline**

|  |  |  |  |
| --- | --- | --- | --- |
| **REG\_IF\_ID(31** – **0)** | **REG\_ID\_EX(82** – **0)** | **REG\_EX\_MEM(55** – **0)** | **REG\_MEM\_WB(36** – **0)** |
| IF.Instruction(31 – 16) | UC.MemtoReg(82) | ID/EX.MemtoReg(55) | EX/MEM.MemtoReg(36) |
| IF.PC + 1(15 – 0) | UC.RegWrite(81) | ID/EX.RegWrite(54) | EX/MEM.RegWrite(35) |
|  | UC.MemWrite(80) | ID/EX.MemWrite(53) | MEM.MemData |
|  | UC.Branch(79) | ID/EX.Branch(52) | EX/MEM.ALURes(18-3) |
|  | UC.ALUOp(78-76) | EX.BranchAddress(51-36) | EX/MEM.outmuxRegDst(2-0) |
|  | UC.ALUSrc(75) | EX.Zero(35) |  |
|  | UC.RegDst(74) | EX.ALURes(34-19) |  |
|  | IF/ID.PC+1(73-58) | ID/EX.RD2(18-3) |  |
|  | ID.RD1(57-42) | Test\_env.outmuxRegDst(2-0) |  |
|  | ID.RD2(41-26) |  |  |
|  | ID.Ext\_Imm(25-10) |  |  |
|  | IF/ID.Instruction(9-6) |  |  |
|  | IF/ID.Instruction(5-3) |  |  |
|  | IF/ID.Instruction(2-0) |  |  |

|  |  |
| --- | --- |
| 1: addi $1,$0,1  2: ori $2,$0,10  3: addi $5,$0,0  4: ori $4,$0,0  5: andi $7,$1,1  6: beq $7,$0,3  7: addi $7,$1,-1  8: sw $7,0($5)  9: j 11  10: sll $6,$1,1  11: sw $6,0($5)  12: lw $3,0($5)  13: add $4,$4,$3  14: addi $1,$1,1  15: addi $5,$5,1  16: beq $1,$2,1  17: j 4  18: sw $4,0($5) | 1: addi $1,$0,1  2: ori $2,$0,10  3: addi $5,$0,0  4: ori $4,$0,0  5: andi $7,$1,1  6: NoOp  7: NoOp  8: beq $7,$0,7  9: NoOp  10: NoOp  11: NoOp  12: addi $7,$1,-1  13: NoOp  14: j 19  15: sw $7,0($5)  16: sll $6,$1,1  17: NoOp  18: NoOp  19: sw $6,0($5)  20: lw $3,0($5)  21: NoOp  22: NoOp  23: add $4,$4,$3  24: addi $1,$1,1  25: NoOp  26: addi $5,$5,1  27: beq $1,$2,5  28: NoOp  29: NoOp  30: NoOp  31: j 4  32: NoOp  33: sw $4,0($5) |

* între instrucțiunea 5 și 6, 7 și 8 , 10 si 11, 12 si 13, 14 si 16 există hazard de tip RAW (după $7, $7, $6 $3, $1); la instructiunile de salt beq si j exista hazard de control

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Nr. Crt.** | **Instruction** | **CC1** | **CC2** | **CC3** | **CC4** | **CC5** | **CC6** | **CC7** | **CC8** | **CC9** | **CC10** | **CC11** | **CC12** | **CC13** | **CC14** | **CC15** | **CC16** | **CC17** | **CC18** |
| 5 | andi $7,$1,1 | IF | ID | EX | MEM | WB  ($7) |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 6 | beq $7,$0,3 |  | IF | ID  ($7) | EX | MEM | WB |  |  |  |  |  |  |  |  |  |  |  |  |
| 7 | addi $7,$1,-1 |  |  | IF | ID | EX | MEM | WB ($7) |  |  |  |  |  |  |  |  |  |  |  |
| 8 | sw $7,0($5) |  |  |  | IF | ID ($7) | EX | MEM | WB |  |  |  |  |  |  |  |  |  |  |
| 9 | j 11 |  |  |  |  | IF | ID | EX | MEM | WB |  |  |  |  |  |  |  |  |  |
| 10 | sll $6,$1,1 |  |  |  |  |  | IF | ID | EX | MEM | WB ($6) |  |  |  |  |  |  |  |  |
| 11 | sw $6,0($5) |  |  |  |  |  |  | IF | ID ($6) | EX | MEM | WB |  |  |  |  |  |  |  |
| 12 | lw $3,0($5) |  |  |  |  |  |  |  | IF | ID | EX | MEM | WB ($3) |  |  |  |  |  |  |
| 13 | add $4,$4,$3 |  |  |  |  |  |  |  |  | IF | ID ($3) | EX | MEM | WB |  |  |  |  |  |
| 14 | addi $1,$1,1 |  |  |  |  |  |  |  |  |  | IF | ID | EX | MEM | WB ($1) |  |  |  |  |
| 15 | addi $5,$5,1 |  |  |  |  |  |  |  |  |  |  | IF | ID | EX | MEM | WB |  |  |  |
| 16 | beq $1,$2,1 |  |  |  |  |  |  |  |  |  |  |  | IF | ID ($1) | EX | MEM | WB |  |  |
| 17 | j 4 |  |  |  |  |  |  |  |  |  |  |  |  | IF | ID | EX | MEM | WB |  |
| 18 | sw $4,0($5) |  |  |  |  |  |  |  |  |  |  |  |  |  | IF | ID | EX | MEM | WB |



* E totul descris in VHDL si nu exista erori.